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would

- a) forming bit line patterns on a substrate including word line patterns, thereby forming a first resulting structure;
- b) forming an interlayer insulating layer on the first resulting structure;
- c) etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening between neighboring bit line patterns; and
- d) forming insulating layers on sidewalls of the bit line patterns.

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A2

6. (Amended) A method of claim 1, wherein top surfaces of the bit line patterns are covered with a layer selected from a group consisting of a silicon nitride layer, a silicon oxynitride layer, and an oxide layer.

A3

8. (Amended) The method of claim 7, wherein in step c), the interlayer insulating layer is etched by using a gas selected from a group consisting of Ar, O<sub>2</sub>, N<sub>2</sub>, H<sub>2</sub>, CH<sub>4</sub>, C<sub>2</sub>H<sub>4</sub>, and C<sub>x</sub>F<sub>y</sub>.

#### REMARKS

By the present Amendment, Applicants cancel claims 10-20 without prejudice or disclaimer of the subject matter thereof, and amend claims 1, 6, and 8. Thus, claims 1-9 are pending.

In the Office Action, the Examiner objected to claims 1, 6, and 16 for containing informalities; rejected claims 8 and 18 under 35 U.S.C. § 112, second paragraph, for containing informalities; rejected claims 1-3 and 11-13 under 35 U.S.C. § 102(e) as anticipated by Duane et al., U.S. Patent No. 6,329,695 ("Duane"); rejected claims 11 and 16 under 35 U.S.C. § 102(b) as anticipated by Cooper et al., U.S. Patent No.

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